Implementation Aspects of the Physical Layer in SpaceWire

Wahida Gasti, Jorgen Ilstad, Farid Guettache, Giorgio Magistrati

ESTEC / European Space Agency, Noordwijk , Netherlands

San-Antonio November 8th 2011

SpaceWire Conference 2011 San-Antonio
Texas US
8-10 November 2011

Introduction

This presentation will focus on the following three areas of the SpW physical layer:

1 -What are the pros and cons of discrete vs. integrated implementation of EIA/TIA 644 LVDS transceivers in flight units?

2-How are fail safe requirements defined in ECSS-E-ST-50-12 verified?

3-How does common mode voltage drift affect communication integrity?

Discrete Versus Integrated Implementation

- *General signal consideration*

-Signal integrity, power-thermal, ESD etc,

- *And more specific to space*

-Redundancy and cross-trapping and risk associated in case of failure

Signal aspect

- Load capacitance
- Power-thermal
- ESD
- Noise
- Technology
  - Gain from radiation tolerance
  - Generation process

PCB issues

- Transmission can suffer from ringing, overshoot, undershoot, crosstalk and reflections.
- LVDS transceiver is integrated into an FPGA/ASIC the possibilities of placement on the PCB are limited

The I/O density in the FPGA

Size of the board i.e. distance between component and connector

PCB layers

Component placement density

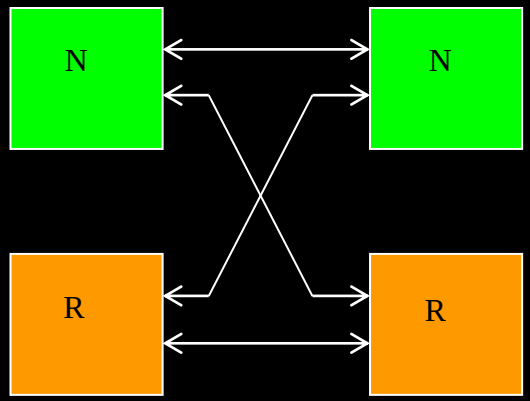
Signal rate.

Redundancy

- In warm redundancy the LVDS driver is always active and the cable can be considered never disconnected from the driver and the receiver input is never shorted
- In cold redundancy the link is not always active and when the driver output is in high impedance and when the transmission line is not shielded noise can be collected

Cross-Trapping

Full cross-strapping of nominal and redundant on-board units.



Failsafe Verification

- **ECSS-E-ST-50-12**

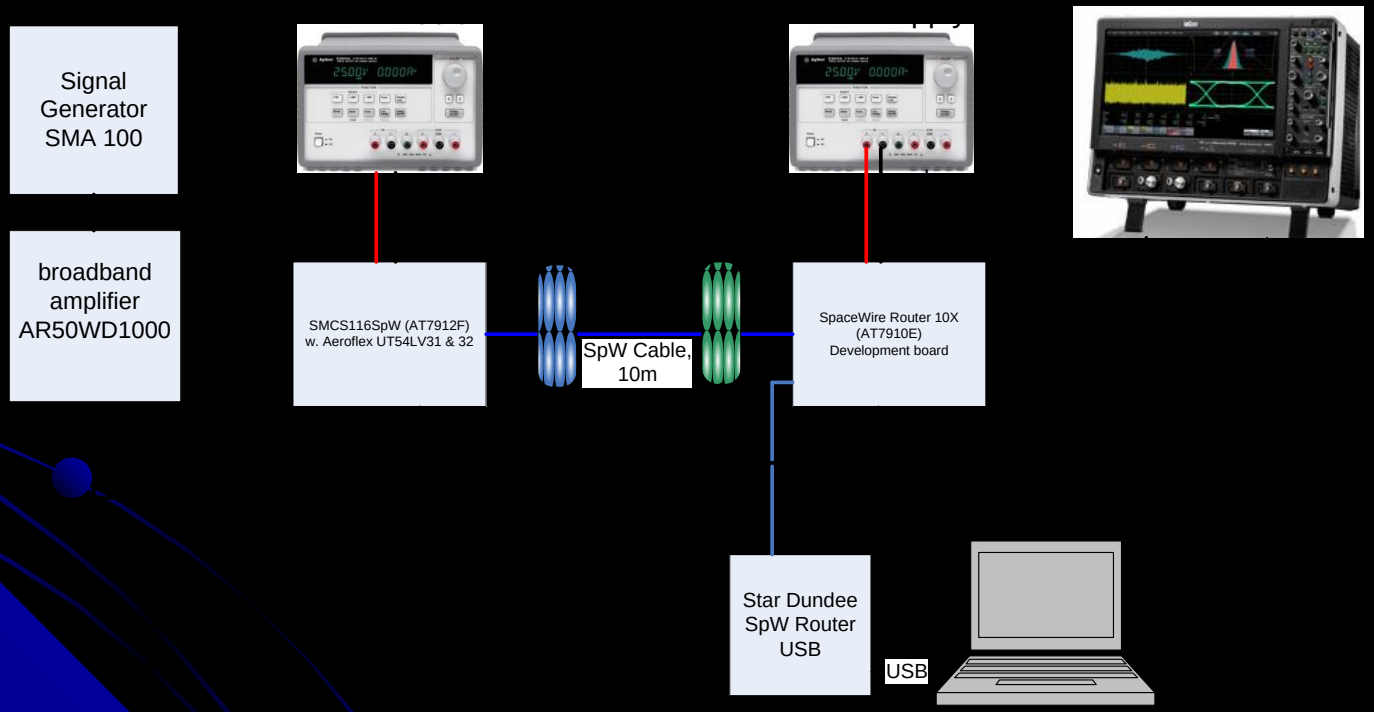
Driver not powered.
Driver disabled.
Driver not connected to receiver
Receiver inputs open circuit (i.e. cable or wire in cable disconnected).
Receiver inputs shorted together

Almost Impossible to verify with IC in particular for ASIC

Common Mode Voltage & Signal Integrity

- Two tests have been carried out
- Voltage injection in the common of the power supply
- EMC test

Test setup description



Common Mode Voltage

- The common of Atmel router SpW interface has been subjected to a voltage variation.
- +/- 1V variation has no impact on data integrity on the SpaceWire link

EMC Test

- Bulk Current Injection Method
- Sine wave with a max amplitude of 1 V in a frequency range of 50kHZ – 100MHz
- SpW link operated at two data rates: 10 Mbit/s and 100 Mbit/s and maintained active
- No perturbation for the injected signal at frequencies lower than 100MHz
- At 100 MHz the shield start to loose its effectiveness

Conclusion

The LVDS standard TIA-EIA-644 requirements are defined with margins that even if fully compliance is not achieved, the LVDS transceivers is able to deliver and decode signals with the required quality level.

Embedded transceivers and discrete circuits have pros and cons, the selection is application dependant, signal integrity is an important metric but at the end it is up to the designer to perform the trade-off.