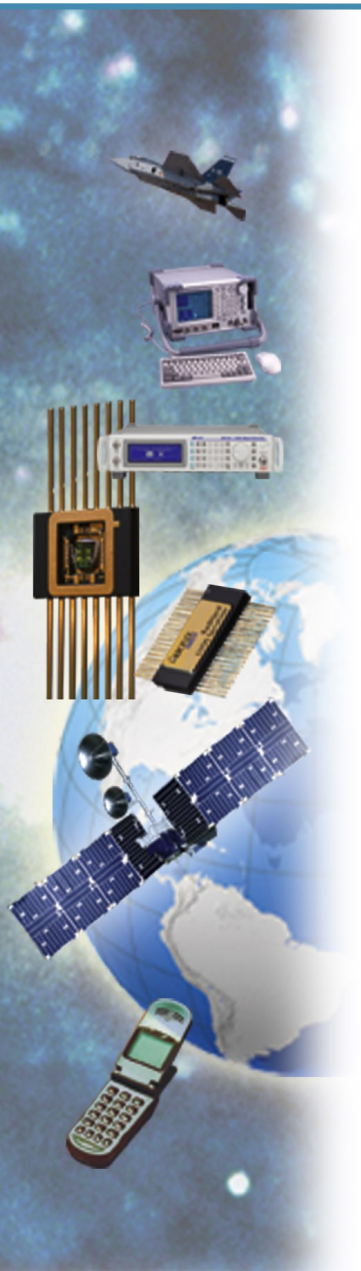

Development of a Novel 18x SpaceWire Router

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Introduction

The 18x SpaceWire router is a new 18 port stand-alone router ASIC component

Currently there are no SpaceWire router components on the world market exhibiting more than eight SpaceWire ports

The goal with this development is to provide this missing key component

The SpaceWire standard (ECSS-E-ST-50-12C) is also evolving with a new revision in the works. The new standard will probably contain features resulting in old devices not being forward compatible

SpaceWire-D (deterministic) is a protocol being developed in parallel with the new standard revision which requires support in routers

This presentation focuses on the architectural and technology choices made for this new ASIC

The impact the new standard revision and the new protocol have on the router design will also be shown

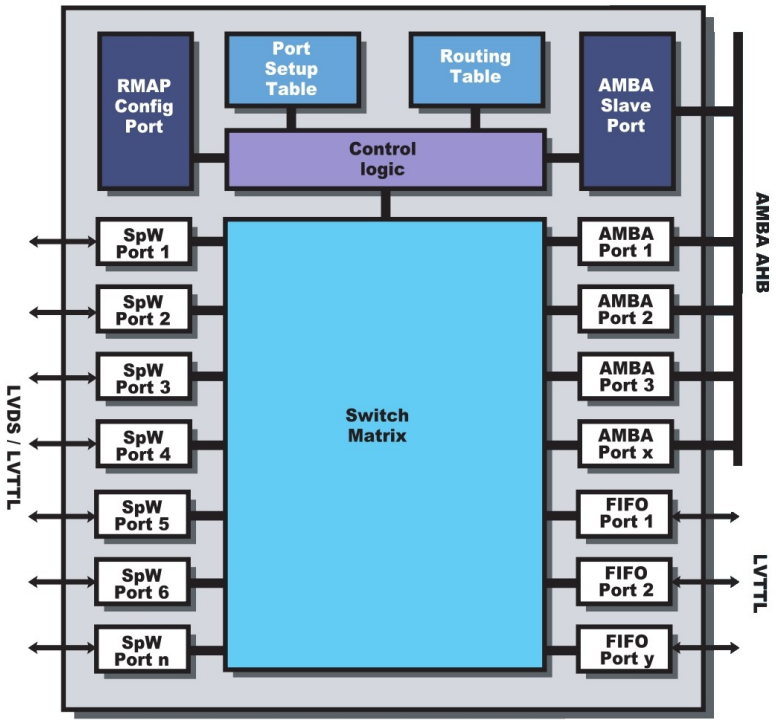
GRSPWROUTER IP CORE

All Aeroflex Gaisler SpaceWire router components are based on the GRSPWROUTER IP core presented at the 3rd International SpaceWire conference in St Petersburg.

The IP core supports everything in the standard including the whole range of ports

Three different port types: SpaceWire links, AMBA AHB DMA interfaces, 9-bit parallel FIFO interfaces

Additional non-standardized features



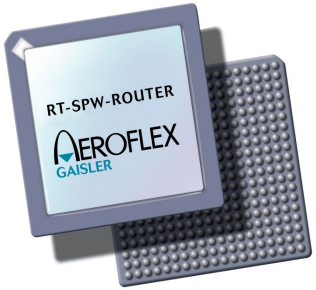
GRSPWROUTER IP Core (2)

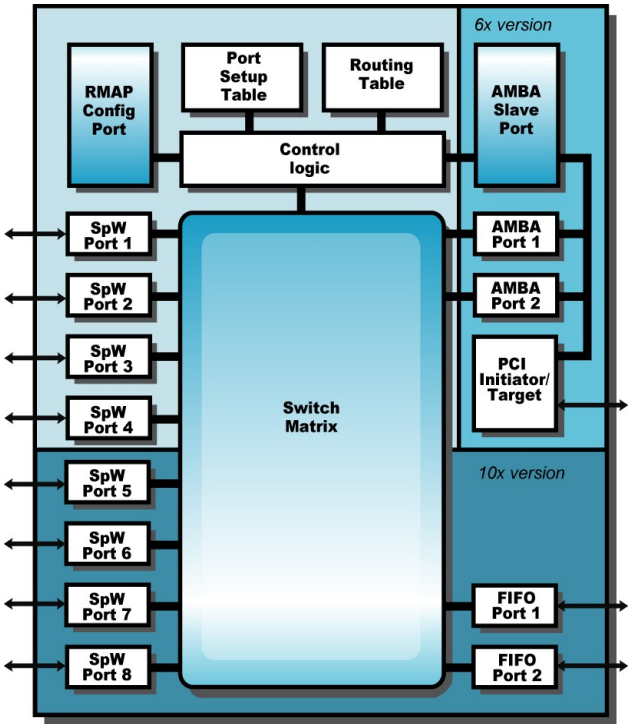
The configurability of the IP core makes it usable in a wide variety of applications.

It has already been used in several Aeroflex Gaisler products.

The RT-SPW-ROUTER rad-hard components on Actel/Microsemi RTAX2000SL and RTProASIC3

Next Generation MicroProcessor (NGMP, meaning of the acronym changing daily) activity funded by the European Space Agency. It is presented in a separate paper at this conference.





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ASIC Requirements

- 16 SpaceWire LVDS ports (choice between LVDS/LVTTL was not obvious)
- 200 Mbit/s link speed (has become an industry standard in practice)
- Some type of additional external interface directly connected to a router port (e.g. AMBA or FIFO port)
- Timer functionality for deadlock prevention (supported by IP-core)
- RMAP based configuration port (supported by IP-core)
- Auxiliary interfaces for diagnostic accesses
- Support for SpaceWire standard revision D (optional)
- Support for SpaceWire-D (optional)
- Low power consumption
- Simple package

ASIC configurations

	Configuration 1	Configuration 2
SpW ports	16 On-Chip LVDS	
RMAP configuration port	Yes	
On-chip AMBA bus	Yes	
AMBA AHB slave port	Yes	
Timers on each port	Yes	
UART, JTAG, SPI and I^2C	Yes	
Auto-scrubbing of routing table	Yes	
SpaceWire LVTTL or FIFO ports	2	0
AMBA AHB ports	0	2
PCI Initiator/Target	0	1

ASIC configurations (2)

18x means the total number of ports, not the number of SpaceWire ports

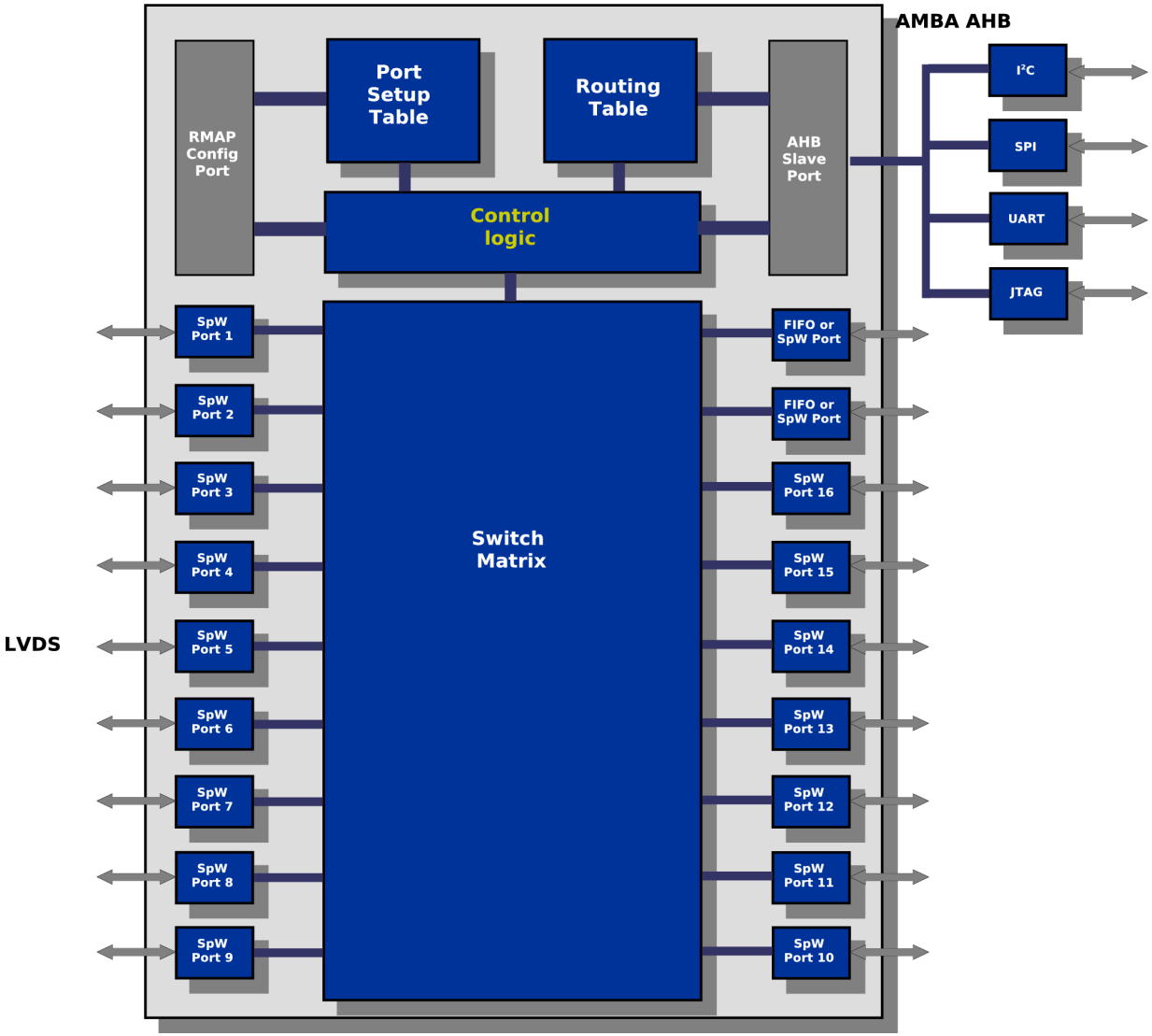
The difference between the two configurations is the type of the two additional ports

Configuration 1 has either two SpaceWire LVTTL or FIFO ports. The decision has not been made which option to choose. The purpose with FIFO ports is to directly connect to parallel interfaces and cascading two routers to achieve more SpaceWire ports. If there is no need to connect to parallel interfaces LVTTL ports are equally suitable for cascading.

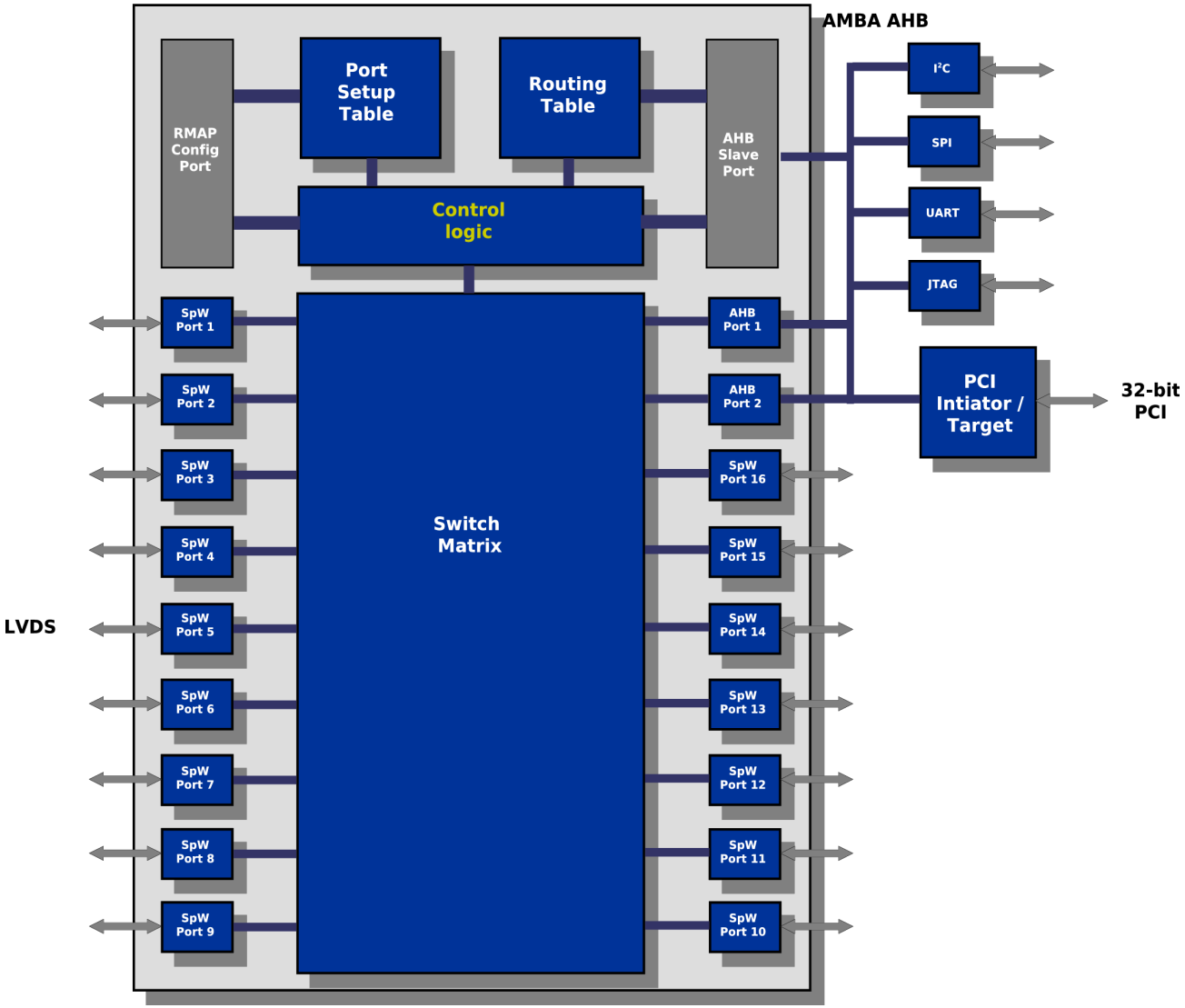
Configuration 2 has two internal AMBA AHB ports connecting to the on-chip AMBA bus which also contains a PCI Initiator/Target. This allows for transferring packets between SpaceWire and PCI

These two alternatives are being evaluated to determine which external interface type is the most useful

Configuration 1 Block Diagram



Configuration 2 Block Diagram



SpaceWire Revision D support

New revision of the SpaceWire standard

Several new features are possibly not backward compatible

Final details of these additions of the standard have not been decided adding considerable risk if they are included in the ASIC

Three changes have been identified as having impact on the implementation:

1. Addition of timers

2. Modification of link-interface FSM

3. Addition of interrupt codes

Timers are already supported in the router and the standard will probably not restrict the way they are implemented so it is anticipated that the current implementation will be compliant

The link-interface FSM modification fixes a rare corner-case which we believe will be backward compatible.

SpaceWire Revision D support (2)

Interrupt codes have a large impact on the router

They require modifications to the SpaceWire codec as well as additional house keeping in the router switch matrix

They are not backward compatible with a lot existing devices

The router could be made a filter where revision D support can be enabled per port. If not enabled the router does not forward any interrupt codes (or other non-supported signaling) to these ports making it possible to have both types of devices on the same network

The big issue is how the schedule of the completion of the new standard revision fits with the schedule of the ASIC. The details might still change adding high risk if added to the router in advance

SpaceWire-D support

Protocol which allows deterministic and low-latency transfers over SpaceWire while simultaneously providing high-bandwidth

Will probably be widely used in the future

Requires a time-slotting table in all units on the network and therefore requires support in the router

Implementation is relatively straight-forward with the current specification

It lacks a time-table for the finalization of the protocol standard

As with interrupt-codes this causes high risk if the router hardware is based on a preliminary specification.

Prototyping

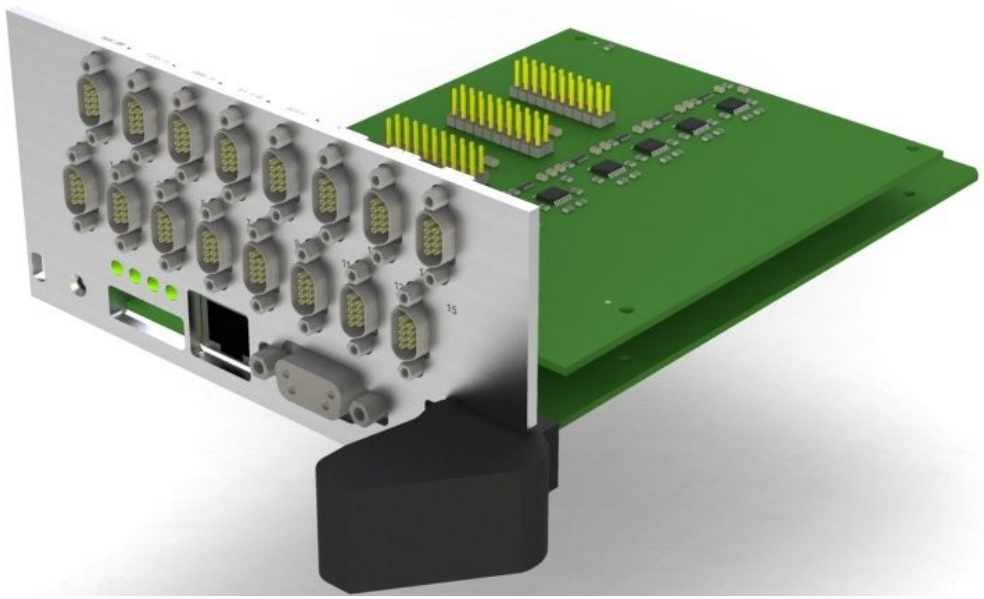
Prototypes for evaluation of the router configurations are already available

Based on Xilinx Virtex4/5 FPGAs

Accompanying development board compatible with RASTA

Board allows interfacing either through PCI, FIFO ports, UART or JTAG

All features (excluding the optional ones) targeted for the ASIC are supported and run at full speed



ASIC Technology and package

The ASIC will be targeted for a 0.18 µm or smaller technology.

Should be SEE free with a TID tolerance of at least 100 kRad

Low power consumption is one of the most important factors

Several candidates have been identified but the actual process and library are yet to be determined

The package is targeted for a simple to handle QFP