SpaceAGE Bus: New Avionics Building Block Concept

Alex Kisin, Glenn Rakow, Eric Gorman

NASA Goddard Space Flight Center
Flight Data System and Radiation Effects Branch
– Custom and/or Euro Card form factor (typically 6U or 3U)
  • Single sided or double sided boards
– Parallel Printed Wiring Board backplane (derived from commercial world)
– Some custom signals added to standard signal set making interchangeability difficult
– All Cards communicate with CPU/Hub through half-duplex interface only one at a time
– Line fault isolation is difficult to achieve because of shared power and bus signals
– No EMI isolation between cards

**Classical C&DH Architecture**

**Signal Buses Traditional Approach: Electrical**

- Isolated Power Converters
- Prime 28V Bus
- Shared secondary voltages bus
- Shared parallel multi-drop half-duplex data bus
Signal Buses Traditional Approach: Connectors

- Hundreds of pins
  - High mate / de-mate forces
  - Stackable connectors are not solderable (lower reliability in vibration)
- Not impedance matched
  - Very difficult to communicate on high speeds
- Difficult alignment and mount
– Custom Enclosure design with card faceplate integrated with card
  • Only 1 available side for user interface connectors
– Wedge locks for card locking and heat dissipation path:
  • Difficult inspection of installed cards: may not be possible at all
  • Possibility of “shaving” wedges during insertion: small metal particles in space
– Fixed distance between cards
  • Problems with tall components or dual side assembly

Wedge lock assembly
- Incompatibility of cards from various vendors
  - Very strong engineering system control is required
  - Some vendors use this to “tie” customers exclusively to their products
  - Sometimes sophisticated rework and redesign is required to match all cards

- Modules are integrated into enclosure are only functionally tested
  - Cards come environmentally untested from vendors: additional testing (EMI/EMC, thermal, vibration) on box level is required
• Create architecture suitable for 90% of space missions
• Reduce costs avionics system development
  – Through significant reduction of Non-Recurring Engineering (NRE)
  – Through standardization of avionic’s electrical and mechanical interfaces
• Simplify electrical interfaces by adopting:
  – Serial communications interface
    • Eliminate mechanical tolerances between backplane connectors and boards
    • Increase system reliability by reducing number of signals
  – Single voltage power distribution
    • Higher voltages to reduce current and eliminate voltage margin concerns
  – Minimal set of commonly used signals
  – Interconnection through a star architecture
    • Common or Central module – HUB
    • Peripheral or User module – NODE
• Simplify mechanical interfaces by adopting:
  – Modular and variable length slot mechanical enclosure concept using card frames (slices) where:
    • Each Printed Wiring Board (PWB) includes its own portion of the mechanical chassis
    • Improvement of thermal design – eliminates wedge locks as thermal path
    • Qualifies modules (slices) for EMI/EMC and thermal requirements
    • Significantly reduces tolerance of mechanical design
Major System Requirements

- High speed communication links
  - Compatibility with high speed (gigabit) serial protocol
- Power distribution
- Reliability
  - module-to-module isolation
  - Support Redundancy schemes
- Ease of implementation
  - Minimal compatibility requirements
  - Simple predefined interfaces
- Ease of expansion
  - Up to 7 NODE modules in same chassis (8 or 9 modules total including HUB module(s))
  - At least 1 surface reserved for user connectors
Proposed SpaceAGE Bus Architecture

- All nodes communicate with the hub concurrently through full-duplex I/F.
- All connections are done through dedicated, fault isolated, differential I/F.
- No shared connections!

Key Points:
- Full-duplex connections and independent power.
- Optional FD connections.

Diagram:
- Spacecraft Avionics
- Peer HUB
- SpaceAGE BUS C&DH

Nodes:
- Node 1
- Node 2
- Node 3
- Node 4
- Node 5
- Node 6
- Node 7
Proposed SpaceAGE Bus System Functions

• **Data**
  - Serial communications from HUB to each NODE
    • Data rates per link: from 1Kbps to up to 3.125Gbps (user configurable and programmable)
    • Differential pairs for Full duplex operations
    • Multiple streams: HUB can talk simultaneously to more than one NODE
    • HUB-to-HUB talk in redundant system architecture
    • Flexible data transfer protocols such as SpaceWire, SpaceFibre, PCI Express, etc: all can co-exist in 1 system
    • AC coupling for better CMV protection

• **Power**
  - 28V bus switched power distribution from HUB
    • Up to 20-30W RMS power per NODE
    • Electrical isolation between Hub(s) and Nodes
    • True “hot” plugging/unplugging for all NODEs and HUBs without disturbing other system components
    • Capability to work directly with 120V power bus voltages

• **Clock**
  - Individually distributed from HUB to each NODE
    • User programmable clock distribution for S/C events synchronization
    • Single frequency power supplies synchronization

• **Analog telemetry**
  - HUB will process all Node telemetry (with 0.1% accuracy); Node requires to have:
    • Either differential multiplexer and signal scale conditioner for NODE analog signals (0.1% accurate), or
    • Single thermistor, if any NODE analog circuitry is undesirable

• **Auxiliary**
  - Facilitate NODE control from HUB
    • Independent reset for each module
    • Single frequency power synchronization
    • Allow true hot plugging/unplugging of each module
Only 16 wires per NODE are needed to transfer all essential bus functions.

If redundancy is required – NODE will get the same wire set from peer HUB.
HUB to HUB Connections

Only 16 wires per HUB are needed to exchange with all essential functions
SpaceAGE Bus Power Distribution

With NODE Isolation

HUB

S/C 28V Power Bus

120-to-28V Non-Isolated Converter

Optional

S/C 120V Power Bus

Prime 28V Bus Voltage

Isolated secondary voltages

Protection

Common EMI Filter

Solid State Relay (SSR)

Isolated HUB Converters

POL's

LDO's

Node 1 SSR Switch

Capacitor Bank*

Node 1

Isolated HUB Converters

POL's

LDO's

Node 7 SSR Switch

Isolated Node 7 Converters

POL's

LDO's

* − in case of power failure provides 200μS of power to save current HUB/Nodes configurations

No DC Chassis connection (AC is OK)

Without NODE Isolation

HUB

S/C 28V Power Bus

120-to-28V Non-Isolated Converter

Optional

S/C 120V Power Bus

Prime 28V Bus Voltage

Isolated secondary voltages

Protection

Common EMI Filter

Solid State Relay (SSR)

Isolated HUB Converters

POL's

LDO's

Node 1 SSR Switch

Capacitor Bank*

Node 1

Non-Isolated Node 1 Converters

POL's

LDO's

Node 7 SSR Switch

Isolated Node 7 Converters

POL's

LDO's

* − in case of power failure provides 200μS of power to save current HUB/Nodes configurations

No Chassis Connection
Proposed SpaceAGE Bus System Summary

• **Ease of implementation**
  – Simple electrical interface
    • Only 16 physical copper wires per link which are capable to satisfy requirements for 90% or more missions
  – Simple mechanical interface
    • Only connectors position is defined
    • No restrictions for module width

• **Much easier compatibility between various vendors**
  – No custom user functions for standardized back connectors

• **Increased data throughput on subsystem level**
  – Serial links will provide higher data rates
  – Double processing/communication rate when 2 HUB modules are plugged in

• **User expandability**
  – Front and Top surfaces are reserved for User connectors
  – Multiple cards per module

• **Lower mass and volume over parallel bus design**

• **Superior heat transfer**
  – Elimination of wedge locks: direct contact between cards and module’s frame
  – Larger contact surfaces between module body and chassis

• **EMI/EMC issues**
  – 100% EMI shielded
  – Lower emitted noise due to a possible total synchronization of all units

• **System reliability**
  – Single string, or
  – Dual independent redundancy, or
  – System cross-redundancy

• **Wide range of applications**
  – Can be used for human or robotic missions
• **Minimum number of conductors**
  – 16, with capability of expansion

• **Wires**
  – Up to AWG#24 wires for power transfer

• **Impedance matching**
  – 100 ohms differential

• **High speed performance**
  – Up to 4 Gbps

• **Shielding**
  – Fully EMI shielded

• **Connectivity**
  – Blind mateable
  – Scoop proofed

• **Material**
  – No vacuum outgassing and weightlessness wiskering

• **Shape**
  – Rectangular for small real estate use
Rugged D-Sub miniature from Sabritec Inc. with Quadraxial pin assembly inserts

4 (shown) and 16 position shells are suggested
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial Communication</td>
<td>Digital</td>
<td>RX+</td>
<td>1</td>
<td>TX+</td>
<td>←</td>
<td>TX+</td>
<td>←</td>
<td></td>
<td>Full Duplex link. Diagonal pins 1-3 and 2-4 provide 100Ω impedance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX+</td>
<td>2</td>
<td>RX+</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>RX−</td>
<td>3</td>
<td>TX−</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TX−</td>
<td>4</td>
<td>RX−</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock and Reset Distribution</td>
<td>Digital</td>
<td>Clock_in+</td>
<td>1</td>
<td>Clock_out+</td>
<td>←</td>
<td>Clock_out+</td>
<td>←</td>
<td></td>
<td>Clock function is defined by Node end user</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset_in+</td>
<td>2</td>
<td>Reset_out+</td>
<td>←</td>
<td>Reset_out+</td>
<td>←</td>
<td></td>
<td>Node can be reset individually by Hub</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Clock_in−</td>
<td>3</td>
<td>Clock_out−</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset_in−</td>
<td>4</td>
<td>Reset_out−</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hub to Hub Bus</td>
<td></td>
<td>Node Power</td>
<td>1</td>
<td>Node Power</td>
<td>←</td>
<td>Node Power</td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power Return</td>
<td>2</td>
<td>Power Return</td>
<td>←</td>
<td>Power Return</td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DC/DC_Sync_in</td>
<td>3</td>
<td>DC/DC_Sync_out</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Power Fail</td>
<td>4</td>
<td>Power Fail</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Telemetry and Node Sense</td>
<td></td>
<td>Analog_out+</td>
<td>1</td>
<td>Analog_in+</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td>Each Node may have 4-16 analog telemetry slots or just 1 passive thermistor; &quot;Sense&quot; tells Hub if Node is plugged in and secured</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Analog_out−</td>
<td>2</td>
<td>Analog_in−</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sense_out+</td>
<td>3</td>
<td>Sense_in+</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sense_out−</td>
<td>4</td>
<td>Sense_in−</td>
<td>→</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cross Communication</td>
<td>Digital</td>
<td>X_TX+</td>
<td>1</td>
<td>X_TX+</td>
<td>←</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Clock_out+</td>
<td>2</td>
<td>X_Clock_out+</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_TX−</td>
<td>3</td>
<td>X_TX−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Clock_out−</td>
<td>4</td>
<td>X_Clock_out−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cross Clock</td>
<td>Digital</td>
<td>X_RX+</td>
<td>1</td>
<td>X_RX+</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Clock_in+</td>
<td>2</td>
<td>X_Clock_in+</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_RX−</td>
<td>3</td>
<td>X_RX−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Clock_in−</td>
<td>4</td>
<td>X_Clock_in−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cross Reset</td>
<td>Digital</td>
<td>X_Reset_out+</td>
<td>1</td>
<td>X_Reset_out+</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peer_Hub_out</td>
<td>2</td>
<td>Peer_Hub_out</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Reset_out−</td>
<td>3</td>
<td>X_Reset_out−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Config_out</td>
<td>4</td>
<td>Config_out</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hub to Hub Plug-in</td>
<td>Digital</td>
<td>X_Reset_in+</td>
<td>1</td>
<td>X_Reset_in+</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Case GND</td>
<td>2</td>
<td>Case GND</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>X_Reset_in−</td>
<td>3</td>
<td>X_Reset_in−</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Case GND</td>
<td>4</td>
<td>Case GND</td>
<td>←</td>
<td></td>
<td>←</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
One of Proposed Routings

Redundant Cross Connections
(only Comm Link is shown)
Suggested HUB Architecture (Digital Section)

**HUB Internal Voltage Telemetry**
- +1.0V
- +1.2V
- +2.5V
- +1.8V
- +1.5V
- +1.0V
- +3.3V

**3.3V Converter Synchronization**
- Node Plug-in Sense
- Peer HUB and ID Sense
- Bank 1: main
- Bank 2: auxiliary
- Bank 3: trial (optional)

**Serial Comm Node Interfaces**
- x7

**Reprogrammable NV Memory w/EDAC:**
- A) Xilinx Configuration
- B) Xilinx CPU ROM
- C) Scratchpad RAM
- 3 banks x 8MB

**FPGA Supervisor:**
- Actel AX2000 or AX4000 with built-in IP cores for:
  - CPU
  - SpW
  - NVRAM programmer, etc.

**Xilinx Virtex-5 FPGA**

**FPGA Bank Configuration:**
- Bank 1: main
- Bank 2: auxiliary
- Bank 3: trial (optional) (8 bits + addr)
- Bank 4

**Serial Comm Functions:**
- a) Full Duplex Comm
- b) Clock Exchange
- c) Mutual Reset

**Node Interfaces:**
- x7

**Node Clock**

**Configuration 8b Slave Bus w/ CRC Check**

**32b Local Bus**

**Bank 1:**
- 256MB SDRAM w/EDAC

**Bank 2:**
- 256MB SDRAM w/EDAC

**Bank 3:**
- 256MB SDRAM w/EDAC

**Bank 4:**
- 256MB SDRAM w/EDAC

**Configuration Bus**

**System Clock**

**POR**

**FPGA Supervisor (Through Analog Card)**

**Peer Hub Communications**

**Node Reset Control (Through Analog Card)**

**External LVDS 4 Ports**

**Flexible S/C Communications**

**External LVDS**

**Serial Comm**

**Hubs Crossover Functions:**
- a) Full Duplex Comm
- b) Clock Exchange
- c) Mutual Reset

**Flexible Debug Communications:**
- UART, 10M Ethernet (Can be also used as S/C General Purpose Communication ports)

**JTAG 1**

**JTAG 2**

**Debug Setup**

**External LVDS**

**GSE Connector**

**2 Ports**

These 4 ports can be configured as:
- a) 4 FD LVDS ports w/ comm rates 1 to 400 Mbps
- b) 2 SpaceWire ports w/ comm rates 10 to 200 Mbps
- c) 4 AC balanced SerDes ports w/ rates 0.15 to 3Gbps
- d) Mixture of all above mentioned port functions
Suggested HUB’s Communication Ports

Front Ports (universal)

SpaceWire Ports (fixed)

Debug Ports (limitedly universal)

HUB

Node Ports (universal)

Peer HUB Port (fixed)

Full Duplex LVDS or CML

Full Duplex LVCMOS

Actel JTAG

Xilinx JTAG

Xilinx Configuration Download

Full Duplex LVCMOS
### Suggested HUB’s Ports Highlights

<table>
<thead>
<tr>
<th>Number of ports</th>
<th>Back (SpaceAGE Bus Ports)</th>
<th>Front (S/C Ports)</th>
<th>Top (mostly for debug)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>8</strong>: 7 NODE(Universal) + 1 Peer HUB</td>
<td><strong>6</strong>: 4 Universal + 2 SpaceWire</td>
<td><strong>2</strong>: Limited Universal</td>
<td></td>
</tr>
<tr>
<td>Physical Interface</td>
<td>Buffered LVDS or AC coupled CML SerDes</td>
<td>Buffered LVDS</td>
<td></td>
</tr>
<tr>
<td>Duplex</td>
<td>Full</td>
<td>Full</td>
<td>Full</td>
</tr>
<tr>
<td>Speed range</td>
<td>1Kbps to 3.125Gbps (up to 100Mbps for SpW)</td>
<td>10Kbps to 100Mbps</td>
<td></td>
</tr>
<tr>
<td>Additional Sync clock</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Protocols</td>
<td>Any type sync or async</td>
<td>Any async + SpW</td>
<td>Async + 10M Ethernet</td>
</tr>
<tr>
<td>In-flight re-configuration</td>
<td>Yes (except Peer HUB)</td>
<td>Yes (except SpW)</td>
<td>Yes (if used for flight)</td>
</tr>
<tr>
<td>State when not used</td>
<td>Hi-Z</td>
<td>Hi-Z</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>Multidrop network use</td>
<td>No</td>
<td>Possible (to 400Mbps)</td>
<td>No</td>
</tr>
</tbody>
</table>
Suggested HUB Architecture (Analog TLM & Power Section)
Suggested NODE Architecture
Assembled System View
Transparent View
L-Bracket Front
Suggested Dual Cards Assembly for HUB Module

2 16x connectors

PCB card 1

Hub's frame

PCB card 2

EMI tight side

EMI tight side

November 8-10, 2011
SpaceWire Conference 2011, San Antonio, TX
Suggested Cross Section View for HUB Enclosure

SPACE FLIGHT CENTER

November 8-10, 2011

SpaceWire Conference 2011, San Antonio, TX
Suggested Layouts for HUB
<table>
<thead>
<tr>
<th>Function</th>
<th>Traditional Buses</th>
<th>Suggested SpaceAGE Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Interface</td>
<td>Parallel</td>
<td>Serial</td>
</tr>
<tr>
<td>Data Exchange</td>
<td>Half-duplex</td>
<td>Full-duplex</td>
</tr>
<tr>
<td>Data Exchange Method</td>
<td>Synchronous</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>Impedance Matching</td>
<td>Mismatched</td>
<td>Matched</td>
</tr>
<tr>
<td>Bus Utilization</td>
<td>Single flow</td>
<td>Multiple independent flows</td>
</tr>
<tr>
<td>Redundancy</td>
<td>Single</td>
<td>Single, Double, Cross</td>
</tr>
<tr>
<td>Power Distribution</td>
<td>Multiple bus voltages</td>
<td>Single voltage</td>
</tr>
<tr>
<td>Bus Current</td>
<td>Medium to very high</td>
<td>Low to very low</td>
</tr>
<tr>
<td>Common Voltage Tolerance</td>
<td>Low (100's of mV)</td>
<td>High (several volts)</td>
</tr>
<tr>
<td>Card-to-Card Isolation</td>
<td>Very complex/Impossible</td>
<td>Possible and very simple</td>
</tr>
<tr>
<td>Hot Plugging/Unplugging</td>
<td>Complex/Impossible</td>
<td>Possible and very simple</td>
</tr>
<tr>
<td>System Telemetry</td>
<td>Not Specified</td>
<td>Standard: Analog &amp; Digital</td>
</tr>
<tr>
<td>EM Interference</td>
<td>Leaking</td>
<td>Fully shielded</td>
</tr>
<tr>
<td>Clock Distribution</td>
<td>Single high frequency</td>
<td>Multiple user defined frequencies</td>
</tr>
<tr>
<td>Clock Skew Requirements</td>
<td>Very tight</td>
<td>Low: not very important</td>
</tr>
<tr>
<td>Connector Pins per Card</td>
<td>Several hundreds</td>
<td>16 per Node plus Chassis</td>
</tr>
<tr>
<td>Bus Interconnect</td>
<td>PCB</td>
<td>Harness</td>
</tr>
<tr>
<td>User Connectors Areas</td>
<td>Front surface only</td>
<td>Front and top surfaces</td>
</tr>
<tr>
<td>PCB Assembly</td>
<td>Single side w/limited back</td>
<td>Dual sided, w/unlimited tier cards</td>
</tr>
<tr>
<td>Card Insertion Force</td>
<td>Medium to high</td>
<td>Low</td>
</tr>
<tr>
<td>Blind Mating</td>
<td>Yes, stress on conn. pins</td>
<td>Yes, stress on conn. metal body</td>
</tr>
<tr>
<td>Scoop Proofing</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Cards or Modules Distance</td>
<td>20-25mm</td>
<td>Limited by communication rates</td>
</tr>
</tbody>
</table>
Questions?